

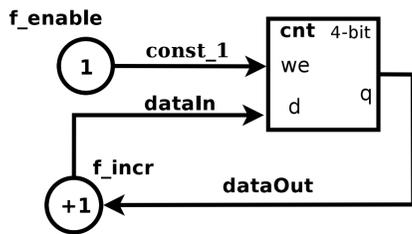
# An Interactive Simulator for Data-flow graphs

*A support tool for s of microprocessor designs.*

*To decrease time and increase quality of the verification process.*

## Input Data-flow Graph

- New input languages can be added



*An example of 4-bit counter model.*

## Internal Simulation Model

- Representation of the input graph
- Basic elements:
  - **Storages** (register or memory)
  - **Functional circuits**
  - **Signals**
- Easy to observe and manage
- Independent of input language

## Simulation Core

- An **efficient simulation algorithm**
- Unnecessary evaluations are **eliminated**
- Can be controlled **interactively**
- Independent of data presentation
- New output interfaces can be added
  - Each can satisfy specific needs

## Simulation Output Presentation

```
$scope module signals $end
$var wire 1 const_1 const_1 $end
$var wire 4 dataOut dataOut $end
$var wire 4 dataIn dataIn $end
$upscope $end
$scope module registers $end
$var reg 4 cnt cnt $end
$upscope $end
$enddefinitions $end

#0
b0000 cnt
b1 const_1
b0000 dataOut
b0001 dataIn

#1
b0001 cnt
b0001 dataOut
b0010 dataIn
```

Value Change Dump (VCD) format

## Textual Output Interface

- Provides direct simulation results in VCD format
- Does not provide interactive tools
- Results can be visualized/analysed by other tools
- Gives a user a simple command-line usage

## Interactive Textual Output Interface

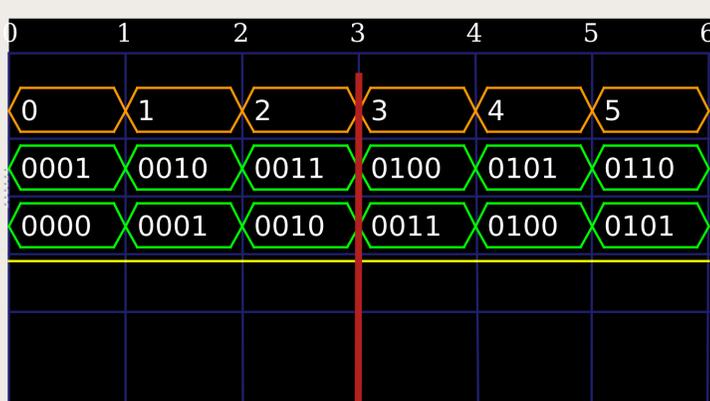
- Also purely textual output interface
- Provides console to enter commands
- Commands can:
  - **control simulation** process
  - **modify/observe state** of a simulated model
- Commands written to a file can be executed repeatedly
- Designed to allow **execution of automated tests** (scripts)

```
>>> init counter.init /* initialize from a file */
>>> step /* perform single simulation step */
>>> dumpreg cnt bin /* Get binary value of register cnt */
0b0000
>>> step
>>> dumpreg cnt bin
0b0001
>>> run 5 /* perform five simulation steps */
>>> dumpreg cnt dec
6
>>> setreg cnt 10 /* Set value of register cnt to 10 */
>>> dumpreg cnt dec
10
```

## Objectives

Name	Value
cnt[0:3]	3
dataIn[0:3]	0100
dataOut[0:3]	0011
const_1	1

## Waves



## Interactive Graphical Interface

- **Visualizes** simulation results and progress
- Helps with **understand** of model's behavior
- Forms robust graphical interface
- Provides the **interactive console**