VERIFIABILITY-DRIVEN SYNTHESIS OF APPROXIMATE ARITHMETIC CIRCUITS USING CARTESIAN GP

APPROXIMATE CIRCUITS PROJECT SUMMARY AND CONTRIBUTIONS aimed at arithmetic circuits - adders and multipliers circuits that do not always perform correct computations work within a certain error in comparison to golden solution error metric - worst case arithmetic error error traded for various circuit metrics integration of two existing methods into one process cartesian genetic programming area approximate circuit evaluation using SAT solvers delay power consumption unique evolutionary strategy - candidates with faster evaluation are preferred motivation: circuit working with 1 % maximal arithmetic error can save up to 90 % of energy **USAGE - ERROR RESILIENT APPLICATIONS** signal and image processing data mining **CORE OF THE EVOLUTIONARY LOOP** neural networks machine learning scientific computing **Algorithm inputs** Algorithm output **RESULTS COMPARISION** Best solution B Seed S Maxima Golden error E solution G previous work results: • up to 8-bit multipliers with error guarantees (full simulation) • up to 16-bit multipliers without error guarantees (random simulation) achieved results: up to 32-bit multipliers ■ up to 128-bit adders with error guarantees **Candidate C** Mutations Parent P (1,2,0) (3,1,1) (0,1,5) (3,2,5) (4,5,2) (1,3,2) (1,2,4) (3,2,1) (0,1,5) (3,2,5) (4,5,2) (1,2,2) Replace parent Candidate evaluation **16-BIT MULTIPLIER COMPARISON** UNSAT Size(C) No Construct Decide(M) in active Size(P) Fail Discard Return 10^{4} 10^{5} 10^{6} 10⁷ 10⁸ Mean absolute error Miter 10^{-3} 10^{-1} 10^{1} 10^{2} Satisfiable? Worst case relative error [%] Bit-width truncation Kulkarni 2x2 [?] EvoApproxLib8 [?] Accurate (*) Proposed methodConfMult16x16Lit [?]ConfMult16x16V1 [?]BSDLC [?]

COMPLEX MULTIPLIERS SYNTHESIS RESULTS

