BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF INFORMATION TECHNOLOGY

Excel@FIT 2025
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Analog Behavioral Modeling for Functional Verification of Mixed-Signal Chips Using SystemVerilog

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Abstract

This paper addresses the challenges of functional verification in mixed-signal integrated circuit (IC) design flows by leveraging high-level behavioral modeling techniques for analog subsystems. Mixed-signal ICs are critical to modern electronic systems, but their verification remains complex and time-consuming. To improve this process, we propose the development of efficient behavioral models that accelerate and enhance functional verification.

Our approach uses SystemVerilog Real-Number Modeling (SV-RNM) to create high-level models of analog subsystems. Integrating these models into the simulation flow streamlines the verification process, significantly speeds up simulations, and facilitates earlier subsystem integration, allowing more bugs to be identified and fixed within the same time frame.

The adoption of behavioral modeling techniques substantially improves the mixed-signal design flow by enabling faster simulations, enhancing communication between analog and digital teams, and reducing costly design iterations. As a result it decreases time-to-market, an essential advantage in the highly competitive semiconductor industry.

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1. Introduction

The increasing complexity of mixed-signal integrated circuits (ICs) demands faster and more efficient functional verification methods. Traditional transistor-level simulations are computationally intensive and often slow down the design cycle. Additionally, the lack of higher-level abstraction and poor communication between analog and digital teams often results in fragmented workflows and increased time-to-market. Our work aims to significantly improve the design flow, and as a result, the verification process for mixed-signal ICs by introducing high-level analog behavioral modeling techniques.

We address the problem of slow and inefficient verification processes in mixed-signal IC design flows. Specifically, we focus on creating high-level behavioral models for analog subsystems that closely replicate real analog behavior while enabling faster simulations. A proper solution should allow early full-chip verification, reduce simulation times, improve team collaboration, and ultimately shorten the design cycle without compromising accuracy.

Traditional mixed-signal verification relies heavily on transistor-level simulations (e.g., SPICE-level), which provide high accuracy but are slow and resource-intensive. Some existing works attempt to introduce higher abstraction levels, but often these models are either oversimplified or do not integrate well with digital verification environments. State-of-the-art approaches include Verilog-A modeling and the use of SystemVerilog Real-Number Modeling (SV-RNM). However, Verilog-A lacks seamless integration with standard digital verification environments, while SV-RNM, although promising, is not yet fully utilized across industry workflows.

We propose using SV-RNM to create analog behavioral models that can be integrated into full-chip UVM-based verification environments. These models replicate the key functional aspects of analog blocks while enabling high simulation speed. Our method also introduces a structured flow where schematic and model updates happen in parallel, fostering better collaboration between analog and digital teams. [1, 2]

2. System Overview and Implementation

We developed a high-level behavioral model of a Li-Ion battery charger, implementing its key operating modes: **Pre-Charge**, **Constant Current Regulation**, **Constant Voltage Regulation**, and**Charge Termination**. These behaviors were captured using SV-RNM constructs, allowing modeling of real-valued signals within a purely digital (discrete) simulation environment.

Furthermore, to validate the concept, we created a simple amplifier behavioral model (Figure 2) that demonstrates how analog signal transformations can be efficiently captured using SV-RNM.

The model simulates the real charging process, as shown in Figure 3 [3] and Figure 5 of the poster. The state transitions follow the Li-Ion battery charging flow depicted in Figure 4, enabling realistic behavior under different conditions and fault events.

The complete workflow (Figure 1) integrates behavioral models early in the verification process, allowing full-chip Universal Verification Methodology (UVM) verification before final analog schematics are frozen.

3. Experimental Results

The use of analog behavioral models led to substantial improvements:

- **Simulation speed-up:** Full-chip simulations with behavioral models ran 10-100× faster compared to mixed SPICE simulations.
- **Early bug detection:** Integrating analog models enabled catching integration issues earlier in the design cycle.
- **Improved collaboration:** Behavioral modeling forced more frequent communication between analog and digital teams, leading to fewer integration surprises.

These results demonstrate the strong potential of analog behavioral modeling, using the SystemVerilog Real-Number Modeling construct, to improve functional verification efficiency and shorten time-to-market.

4. Conclusions

This work highlights the importance of adopting high-level behavioral modeling in the functional verification of mixed-signal ICs. By leveraging SystemVerilog Real-Number Modeling, we enable faster and more comprehensive verification processes, improve interdisciplinary collaboration, and reduce overall development time.

Acknowledgments

I would like to thank my supervisor Ing. Marcela Zachariášová Ph.D., for her guidance and support throughout this project.

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