Analog Behavioral Modeling for Functional Verification of Mixed-Signal Chips Using SystemVerilog

Kirill Shchetiniuk, 2025

Supervisor: Ing. Marcela Zachariášová Ph.D.

Mixed-Signal Challenges

- **Limited Abstraction Levels**: The absence of higher-level abstraction methods significantly hampers design flow efficiency, particularly in complex systems.
- **Prolonged Simulation Times**: Transistor-level simulations require extensive computational resources, making the design verification phase time-consuming and resource-intensive.
- **Misaligned Design Strategies**: Employing unsuitable design approaches often leads to delays and extends time-to-market.
- **Interdisciplinary Communication Gaps**: Poor collaboration between analog and digital teams results in fragmented workflows and limits design integration quality.

Employing New Approaches

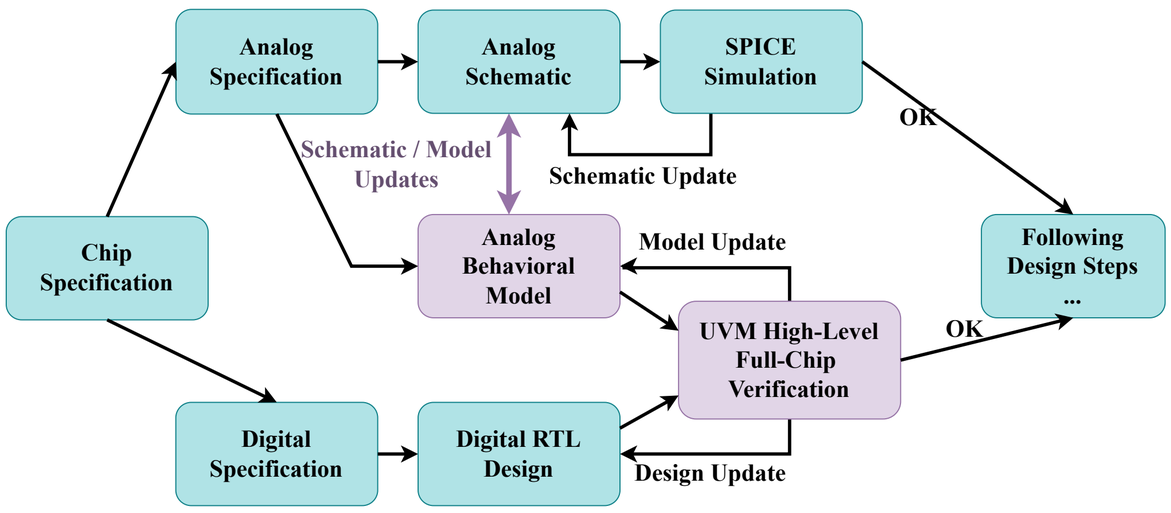
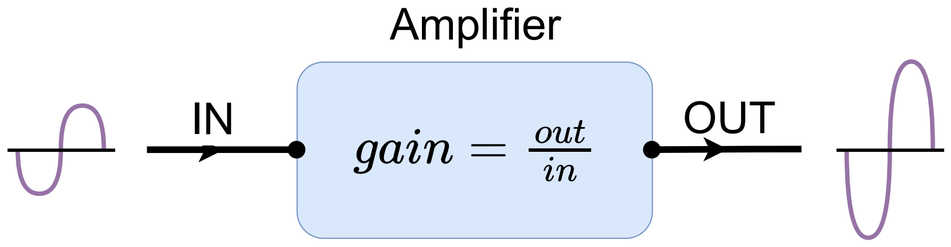


Figure 1. Workflow with Behaviour Models Integration

Adopting novel design approaches with analog behavior models enables higher abstraction levels, allowing to perform fasters simulation, and improves teams collaboration.

SystemVerilog Behavior Modeling




```
module AmplifierRNM (
    input  real analog_in,  // Input signal
    output real analog_out  // Output signal
);

    // Parameters for signal processing
    parameter real gain = 2.0;
    parameter real offset = 0.5;

    // Continuous assignment for signal transformation
    assign analog_out = (analog_in * gain) + offset;

endmodule
```

Figure 2. Amplifier Implemented using SystemVerilog RNM Construct

Employing Behavioral Models in Real Project

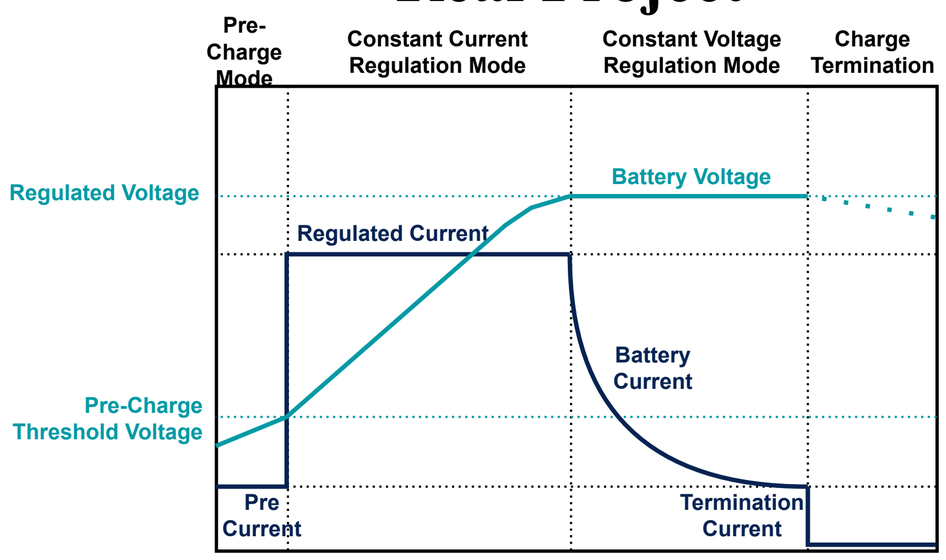


Figure 3. Li-Ion Battery Charging Flow [1]

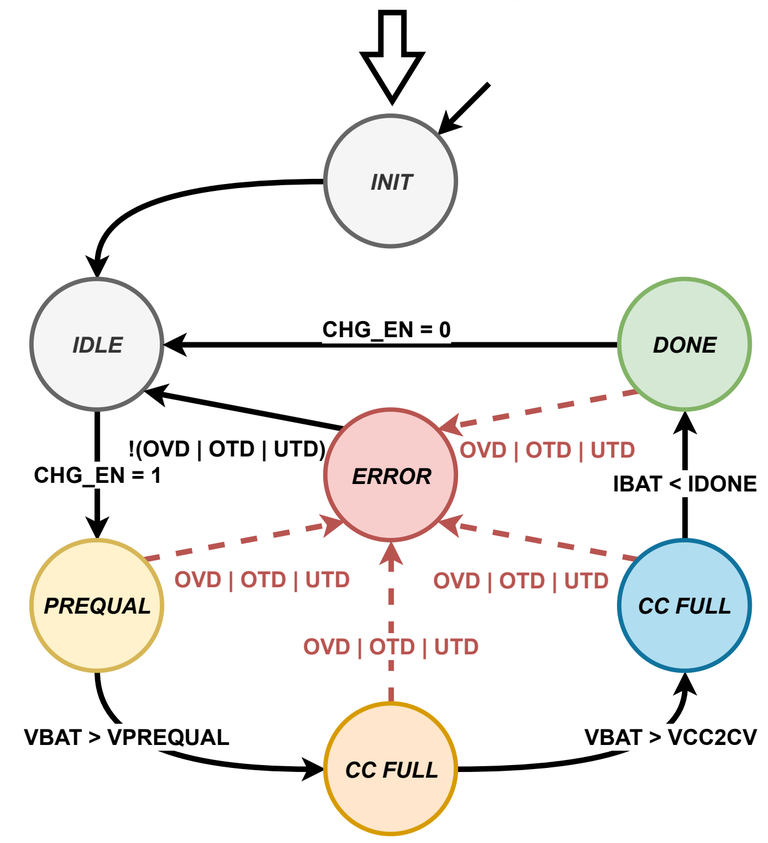


Figure 4. Li-Ion Charger State Flow Diagram

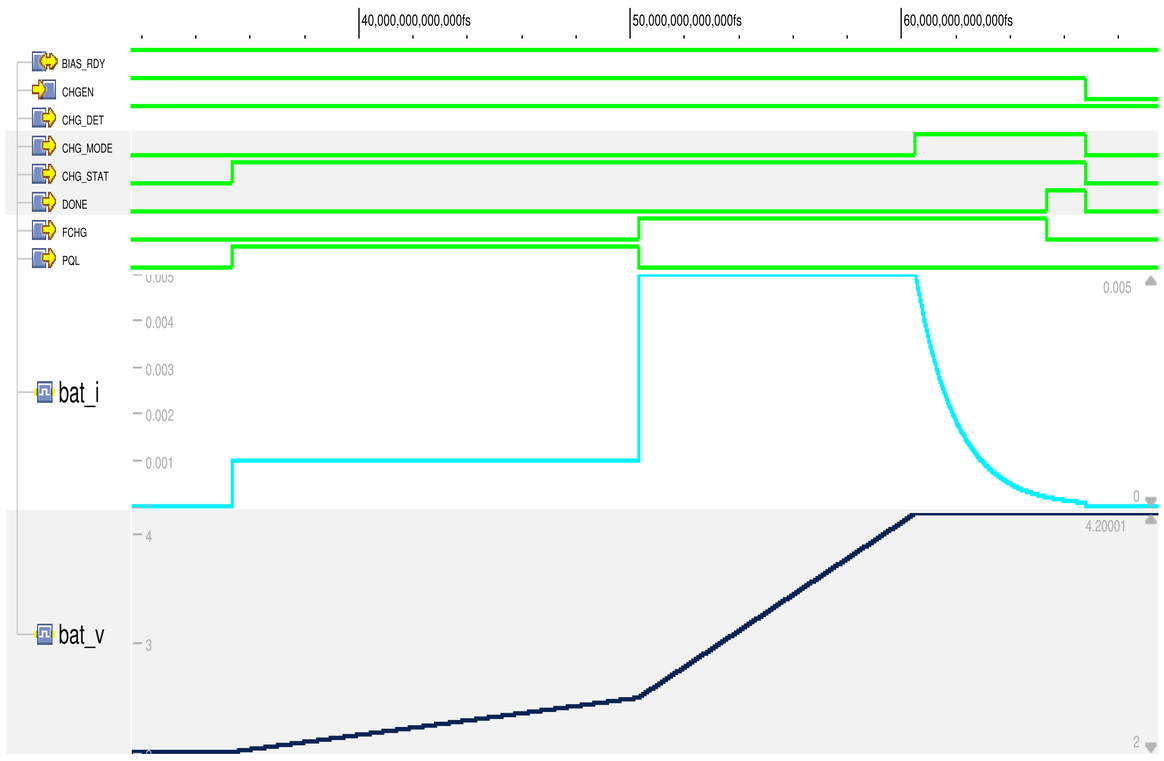


Figure 5. Charging Simulation Waveforms

[1] Mike. *What are the 3 stages of lithium battery charging?*, December 2019. Available at: https://www.grepow.com/blog/what-are-the-3-stages-of-lithium-battery-charging.html