BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF INFORMATION TECHNOLOGY

Excel@FIT 2026
http://excel.fit.vutbr.cz

Design and Implementation of a Low-Cost FPGA-Based Educational Kit

Bc. Filip Masár

Abstract
This paper presents a low-cost, integrated platform for teaching digital hardware design using hardware description languages. The proposed solution consists of a compact FPGA-based board with essential peripherals and a supporting software tool that simplifies synthesis workflows and ensures reproducibility. Compared to existing educational platforms, the proposed system significantly reduces unit cost, enabling deployment on a per-student basis while maintaining sufficient functionality for practical tasks. The platform emphasizes ease of use and reduced complexity, making it suitable for introductory courses. Prototype boards have been successfully tested and has been introduced in pilot teaching, with full integration into the curriculum planned for the upcoming academic year. The results demonstrate that the proposed approach provides an accessible and effective solution for hands-on hardware education.

*xmasar18@stud.fit.vut.cz, *Faculty of Information Technology, Brno University of Technology*

1. Overview

One important aspect of education at BUT FIT is learning about hardware and chip design. This part of the curriculum presents a challenge due to the need for specialized teaching hardware, which is either difficult to obtain or expensive.

Previously, courses used the FITkit [1] (MCU and FPGA), but software support for it gradually declined, so courses shifted to the PYNQ-Z2 board [2] (SoC with CPU and FPGA). However, this board lacks sufficient peripherals for teaching purposes, requiring the development of an external module with an LED matrix. The price of the board itself is also an issue, as it costs around €200 (4,000 CZK).

For these reasons, a new educational board emphasizing low cost and ease of use is proposed. This new board contains only an FPGA and the necessary user peripherals, such as an LED matrix, RGB LED and buttons. The solution was expanded further to include simple software that ensures the reproducibility of the configuration according to the project settings.

The proposed solution costs as little as €26.50 (650 CZK) per unit (when producing 20 units) and provides an easy-to-use option for teaching hardware description languages in the IVH course.

2. Hardware

When selecting an FPGA, we considered the affordability of the chip and the usability of the included design software, including synthesis speed and disk space requirements. The iCE40 UltraPlus FPGA (iCE40UP5K) from Lattice Semiconductor best met these requirements [3]. This FPGA series has the advantage of having unofficial open-source synthesis tools and a large number of open-source PCB designs available. The design was based on one such design: UPduino [4].

The basic architecture of the proposed solution consists of an FPGA, a bitstream programming section, and user peripherals. Figure 1 shows the block diagram of the proposed solution.

An LED matrix was chosen for the primary user interface because it offers sufficient complexity to teach basic timing issues in FPGAs due to its multiplexed control. Another advantage of the LED matrix is that it provides more engaging feedback during implementation than a few status LEDs would.

Five buttons are used for user input and are arranged as four directional buttons and one confirmation button.

Another peripheral is an RGB LED connected to an IP core in the FPGA that is designed to control it. This enables training in working with a specific IP core.

The board includes an FTDI USB-to-SPI converter that facilitates communication between the computer, FPGA, and SPI flash memory. Due to the limited number of flash memory rewrites and the limited write speed, the bitstream is loaded directly into the FPGA's volatile memory. To permanently store the bitstream, the board can be equipped with flash memory.

The default settings allow communication between the computer and FPGA while the system is running. This opens up possibilities for other types of applications that require communication, such as implementing primitive accelerators.

The board features a dual-row connector with a power supply and eight I/O pins from the FPGA to enable future expansion and connection of peripherals.

Because students have the freedom to create the hardware description, forbidden states could arise when controlling the LED matrix. To prevent this, each column is controlled via a decoder (Figure 2), which prevents multiple columns from being activated at once. This protects the solution from potential overload caused by simultaneously activating two or more columns. Current regulators then control individual rows to ensure uniform brightness.

3. Software

The official tools, Lattice Radiant and QuestaSim, are used for synthesis and simulation. Due to the small FPGA, Lattice Radiant software provides much faster and simpler synthesis than the currently used AMD Vidado software. It also requires less disk space, making it easier for students to install.

To simplify using these tools, especially on a server without a GUI, a support tool was created that encapsulates them. In addition to simplifying the process, the support tool provides configurations for individual projects, enabling clear reproducibility of solution synthesis. The current IVH course solution involves submitting projects from the design tool. However, this method may introduce unwanted changes or absolute paths to source files.

Therefore, there will be no need to submit projects from Lattice Radiant; only modified source files need to be submitted. The support tool will then automatically create the project in Lattice Radiant. Figure 3 shows the simplified data flow of the software part.

Another key feature of the utility is its simple, text-based user interface (TUI), which allows users to operate the utility without knowing command-line arguments. The TUI was chosen to support running the utility on a remote server via SSH, eliminating the need to transfer graphical windows.

4. Results

Prototypes of the designed board were created and all of its components were tested and found to function properly. (Figure 4)

The unit price depends on the total number of units produced due to fixed setup costs. When producing 20 units, the unit price was €26.50 (650 CZK). This is significantly less than the previous solution.

Four example tasks were created to demonstrate possible applications. Each task utilized approximately 300 LUTs, except for the Game of Life, which utilizes approximately 1,300 LUTs due to fully parallelized calculation. (Figure 5)

The selected FPGA has 5,000 LUTs and is therefore large enough for simple tasks in an educational environment.

The proposed boards are already being used in pilot testing for the IVH course and are expected to be fully adopted next academic year.

5. Conclusion

The proposed solution is a comprehensive, ready-to-use platform for learning hands-on digital circuit design using hardware description languages.

The platform is priced eight to ten times lower than current solutions, enabling larger-scale deployment and providing access to every student.

The integration of hardware and software makes the platform user-friendly and allows students to quickly learn how to operate it.

Acknowledgements

I would like to thank my supervisor Ing. Vojtěch Mrázek, Ph.D. for his help.

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